

Fig. 1A

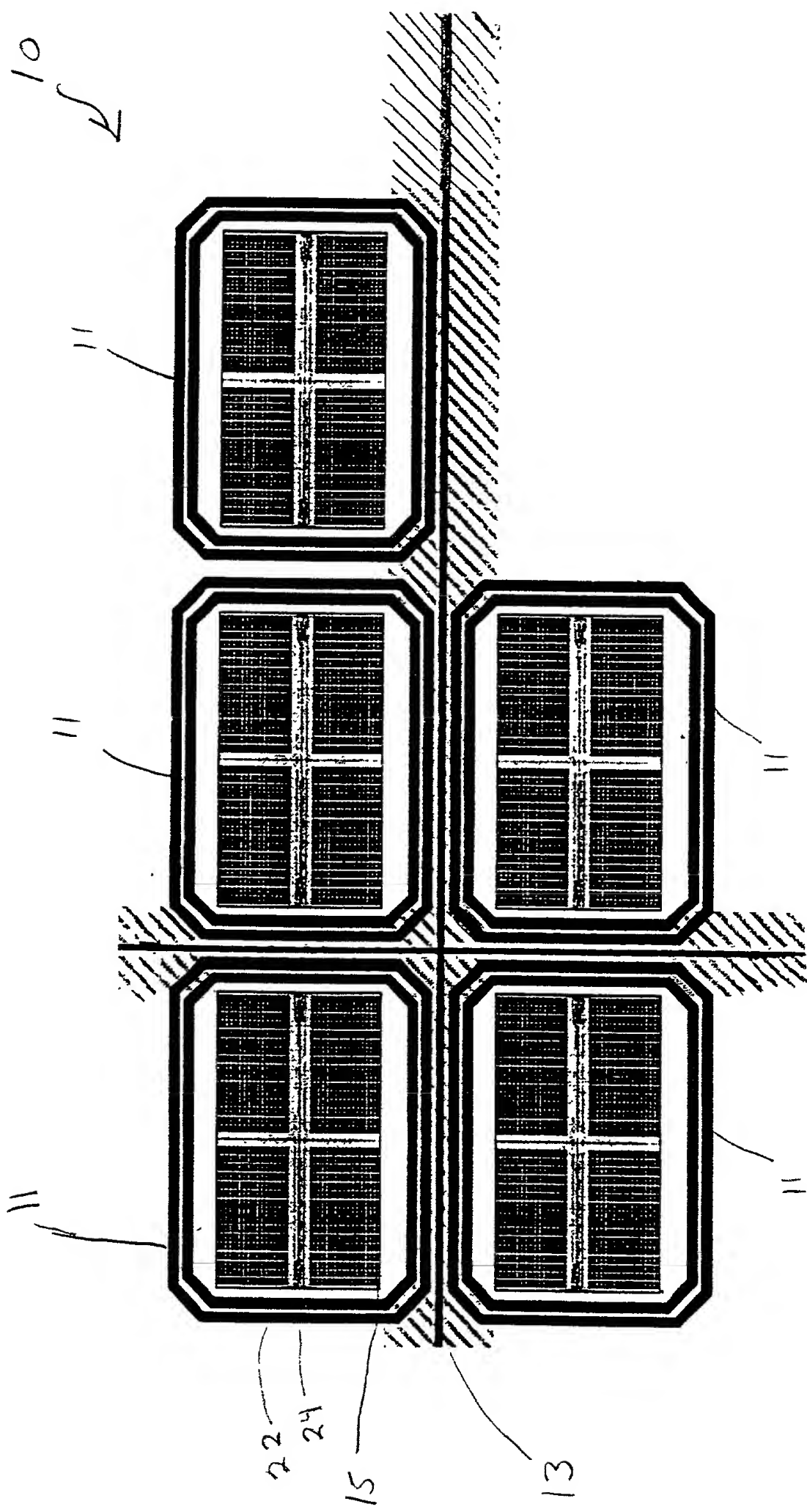


Fig. 1 B

Fig. 2 is a cross-sectional view of the device of Fig. 1, taken along line 2-2 of Fig. 1, showing the device in a first state of operation. The device includes a substrate 10, a first layer 18, and a second layer 24. The first layer 18 is formed on the substrate 10, and the second layer 24 is formed on the first layer 18. The second layer 24 includes a plurality of openings 28, 30, 32a, 32b, 32c, and 32d. The openings 28, 30, 32a, 32b, 32c, and 32d are formed in the second layer 24, and the openings 28, 30, 32a, 32b, 32c, and 32d are in communication with the first layer 18. The openings 28, 30, 32a, 32b, 32c, and 32d are formed in the second layer 24, and the openings 28, 30, 32a, 32b, 32c, and 32d are in communication with the first layer 18. The openings 28, 30, 32a, 32b, 32c, and 32d are formed in the second layer 24, and the openings 28, 30, 32a, 32b, 32c, and 32d are in communication with the first layer 18.

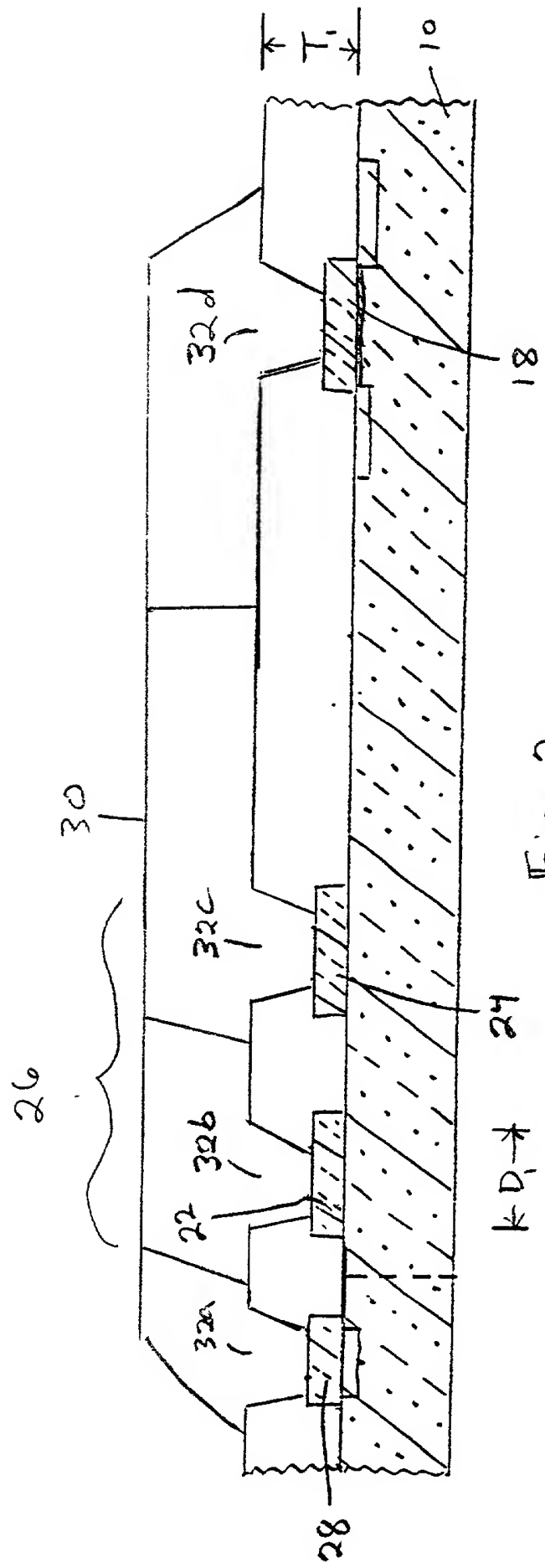


Fig. 2

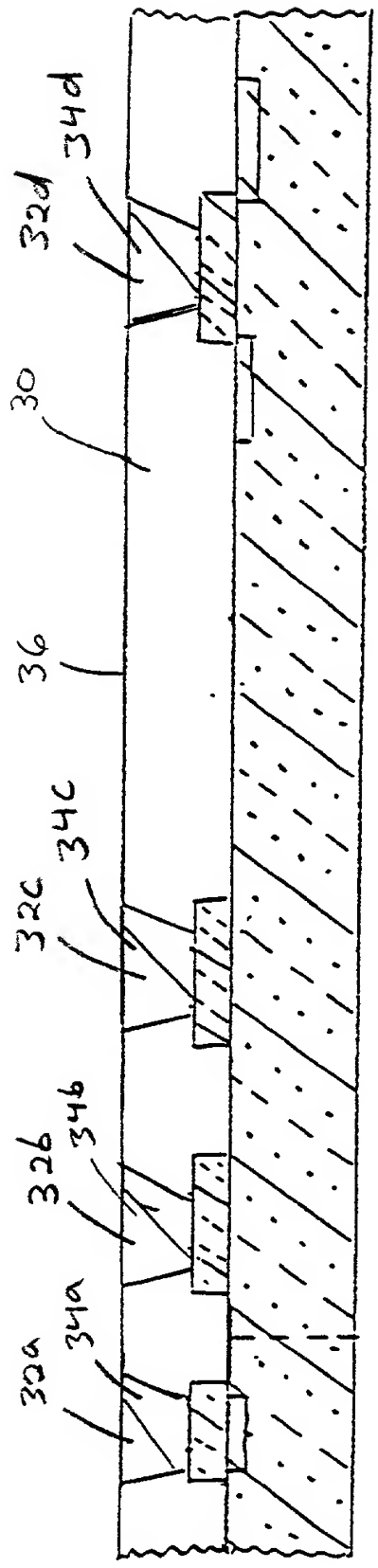


Fig. 3

1. The present invention relates to a method of forming a thin film on a substrate, and more particularly to a method of forming a thin film on a substrate by a chemical vapor deposition (CVD) process.

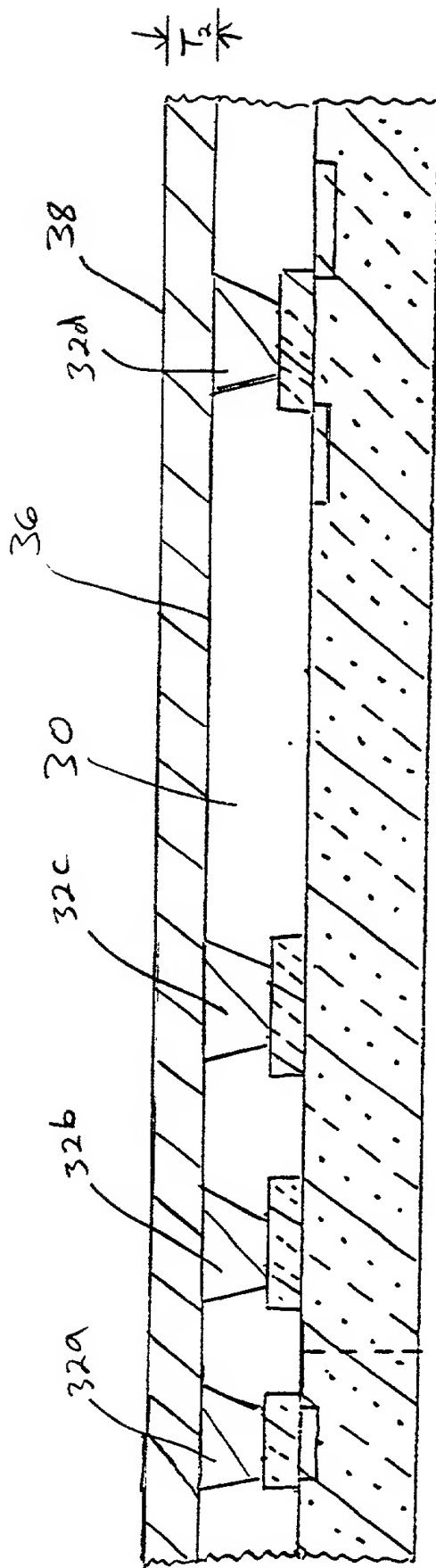


Fig. 4

FIG. 5 is a cross-sectional view of a semiconductor device in accordance with the present invention.

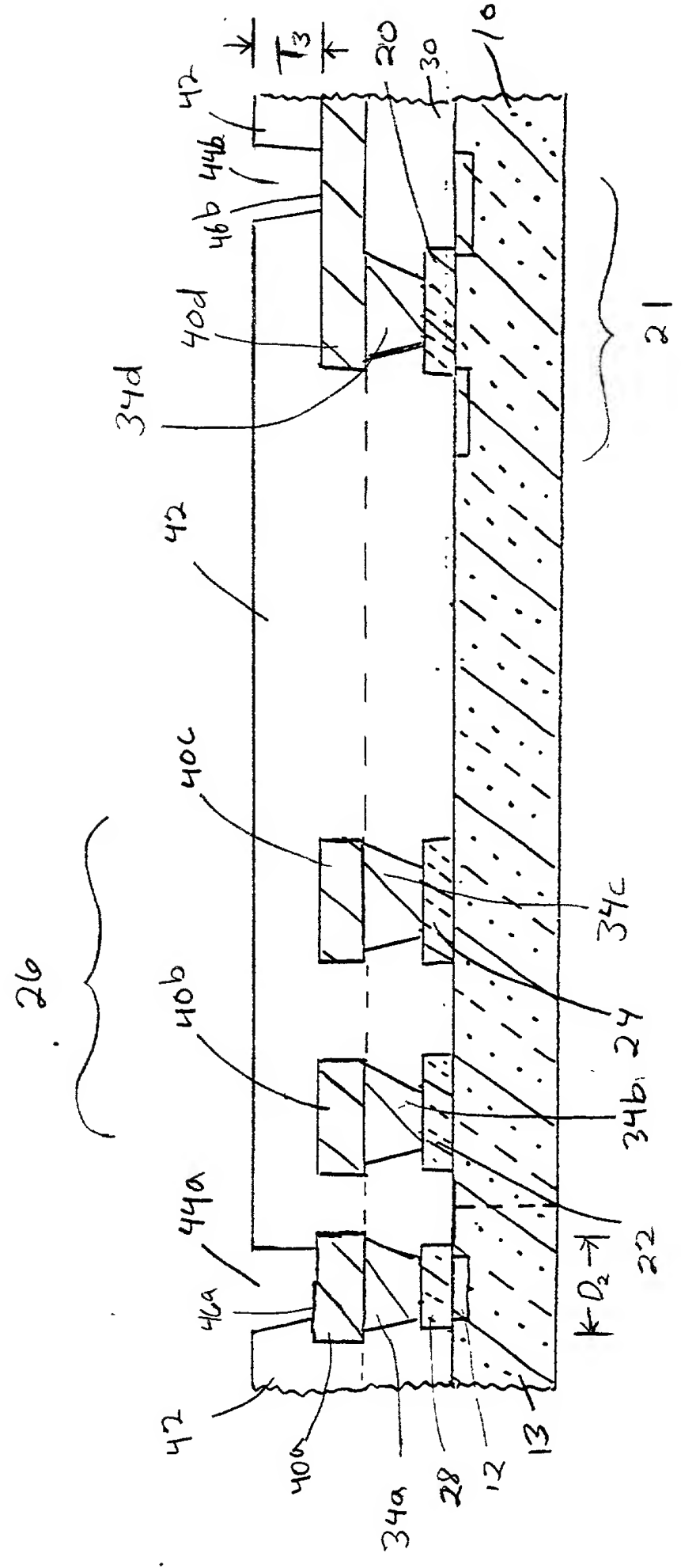


Fig. 5

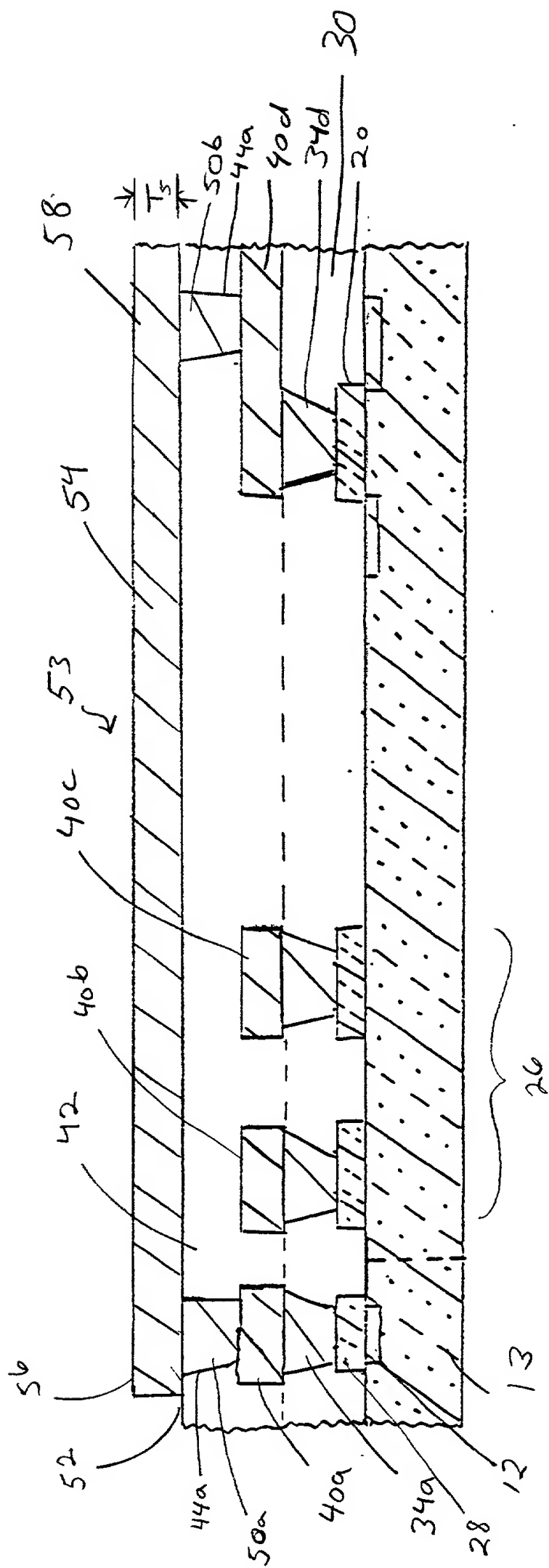


Fig. 6

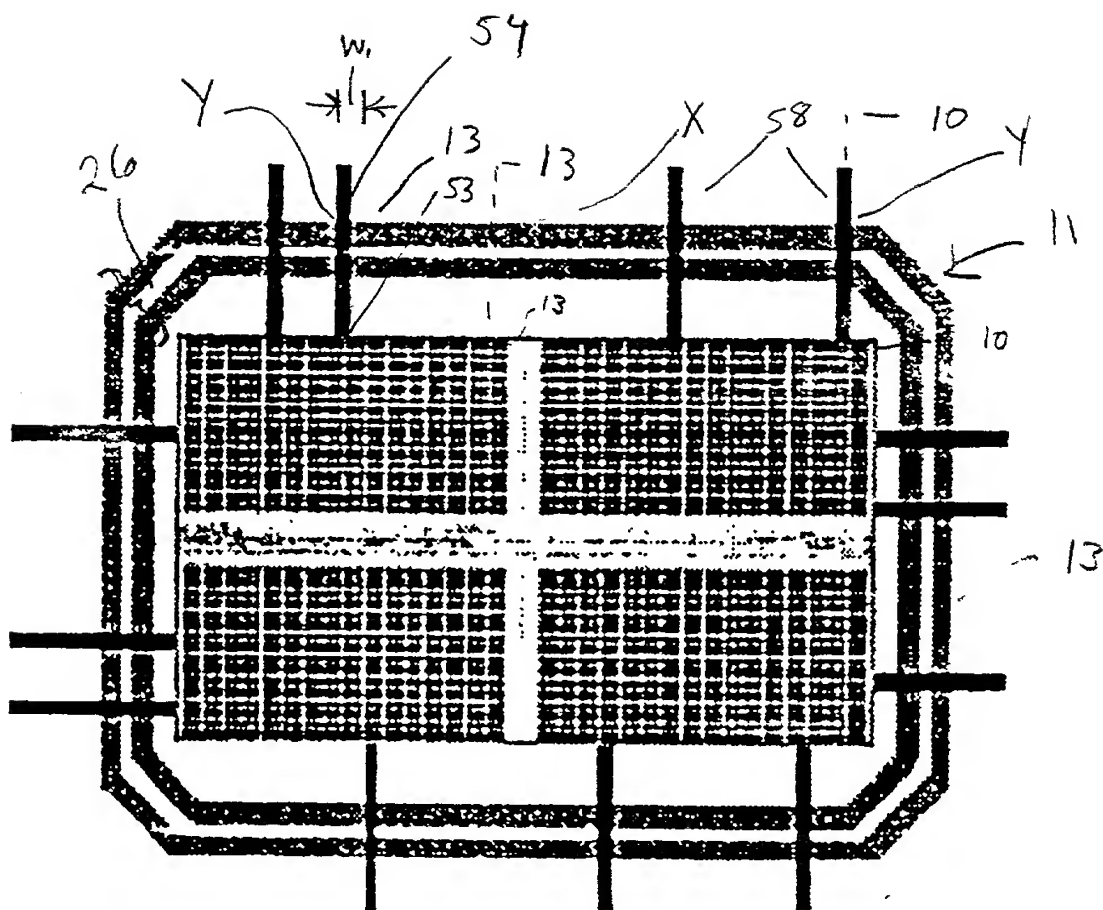


Fig. 7



FIG. 8 is a cross-sectional view of the device of FIG. 7, taken along line 8-8 of FIG. 7, showing the device in a second state of operation. In this state, the device is configured to receive and process a second input signal. The input signal is received by the input port 40 and is processed by the processing unit 42. The output of the processing unit 42 is then sent to the output port 44. The device is configured to receive and process a second input signal, which is different from the first input signal. The device is configured to receive and process a second input signal, which is different from the first input signal. The device is configured to receive and process a second input signal, which is different from the first input signal.

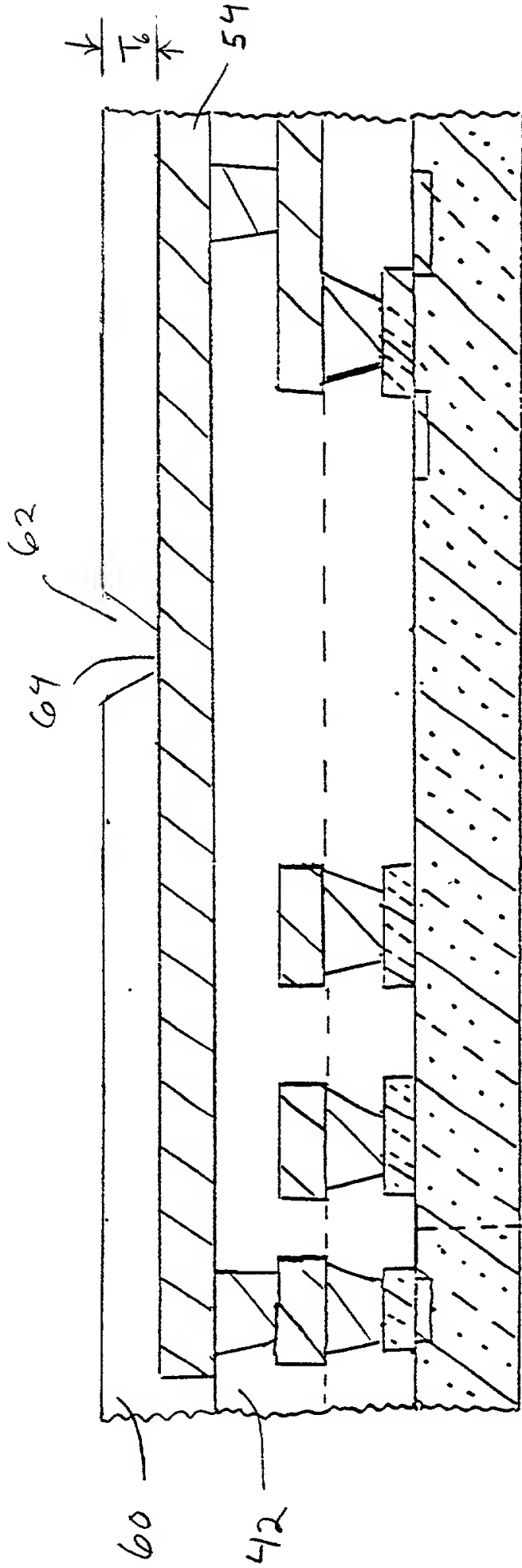


Fig. 8

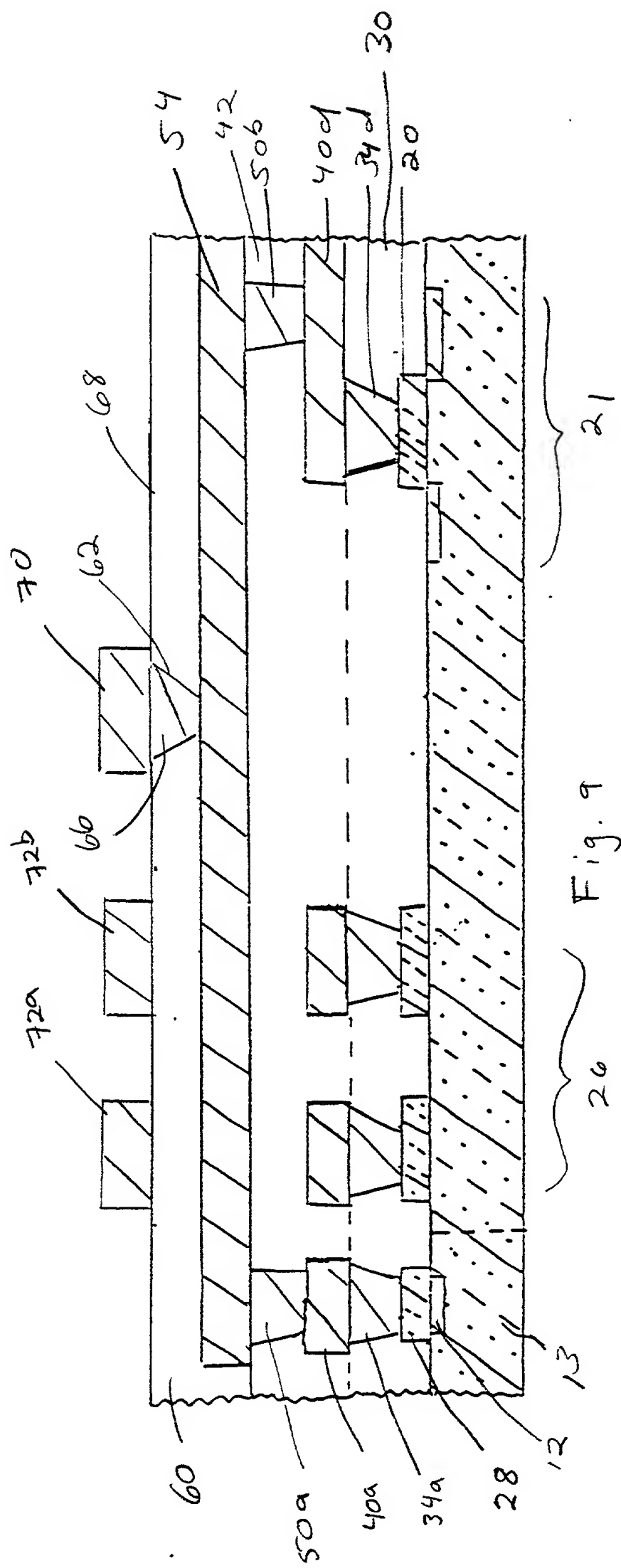


FIG. 10 is a cross-sectional view of a semiconductor device in accordance with the present invention. The device includes a substrate 13, a gate stack 26, and a source/drain region 21. The gate stack 26 includes a gate dielectric layer 30, a gate electrode layer 42, and a gate spacer layer 50b. The source/drain region 21 includes a source/drain dielectric layer 54, a source/drain electrode layer 60, and a source/drain spacer layer 74. The device also includes a contact layer 56, a contact electrode layer 50a, a contact spacer layer 40a, and a contact dielectric layer 34a. The device is formed on a substrate 13.

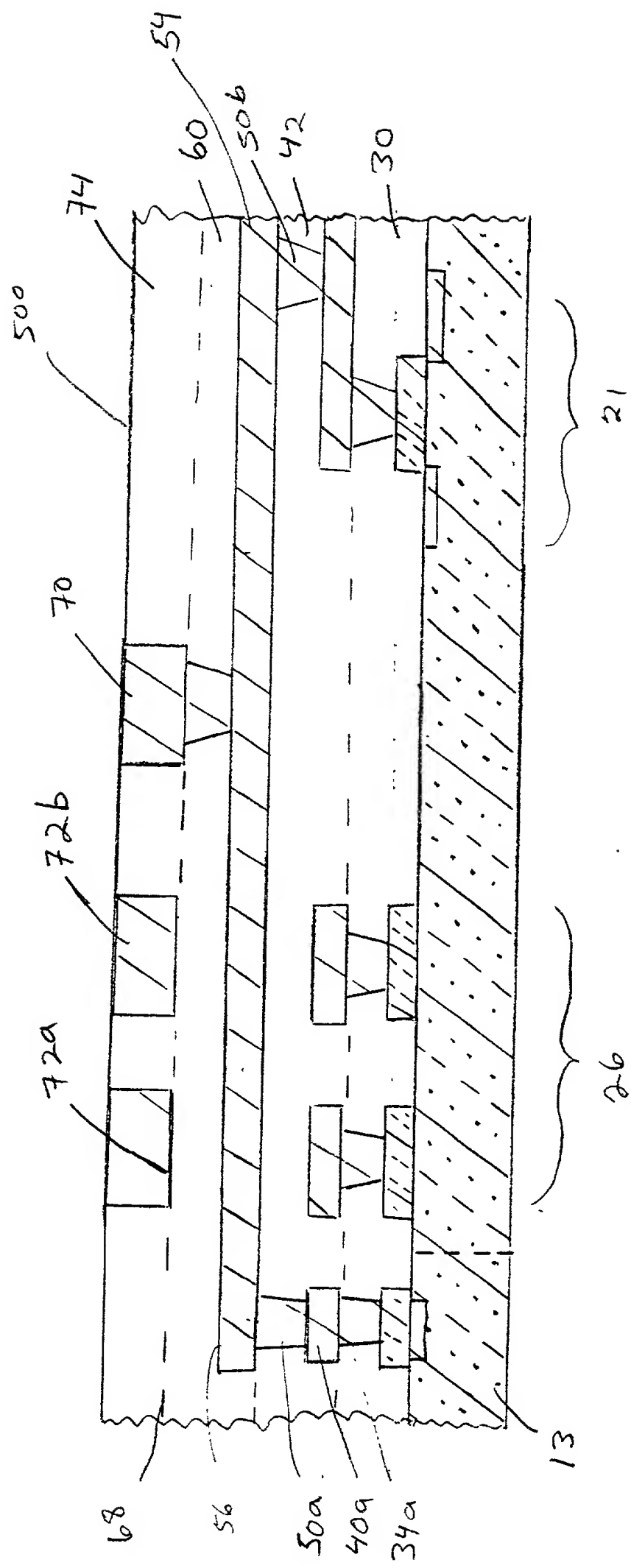


Fig. 10

Fig. 11 is a cross-sectional view of the device of Fig. 10, showing the device in a second state of operation. In this state, the device is in a second state of operation, and the device is in a second state of operation.

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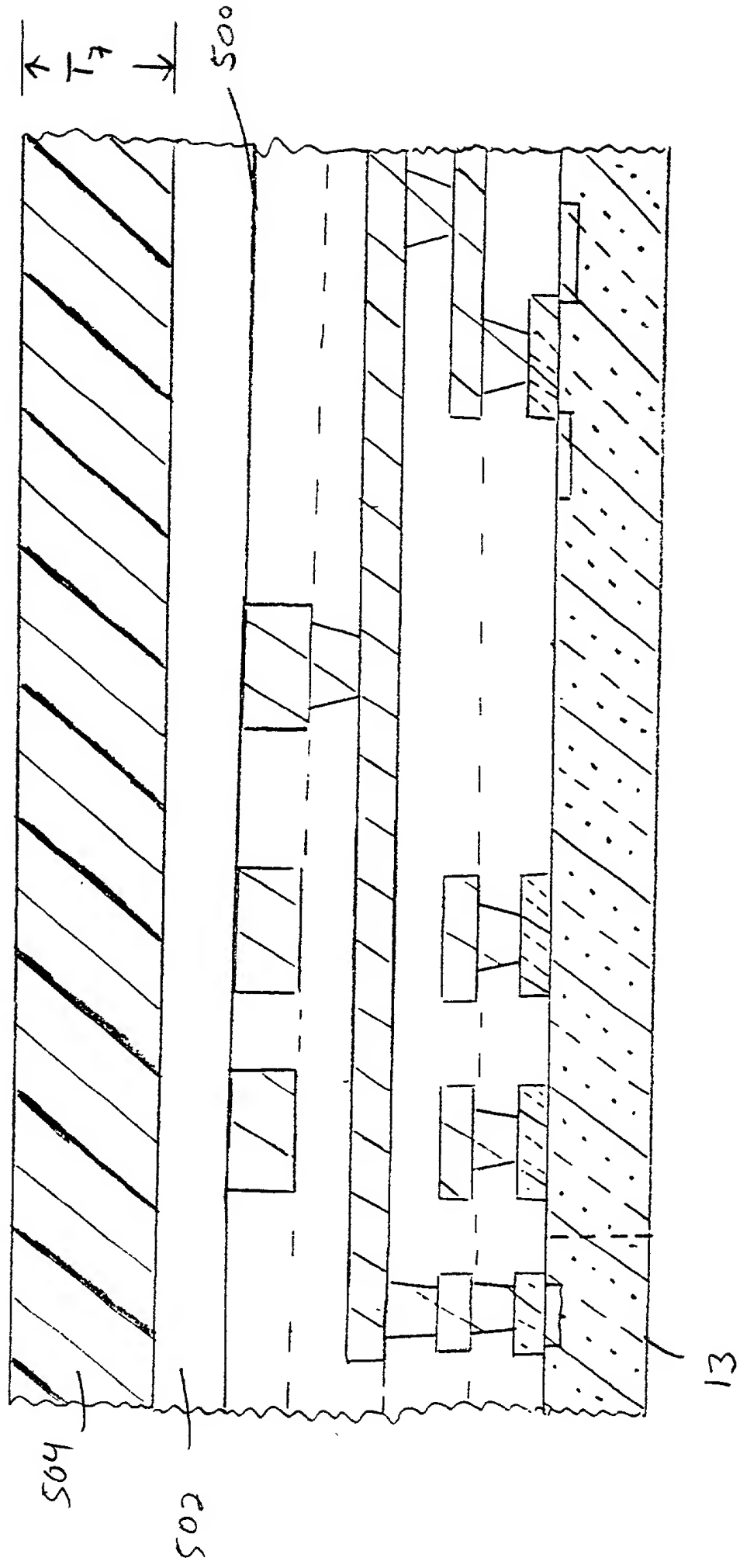


Fig. 11

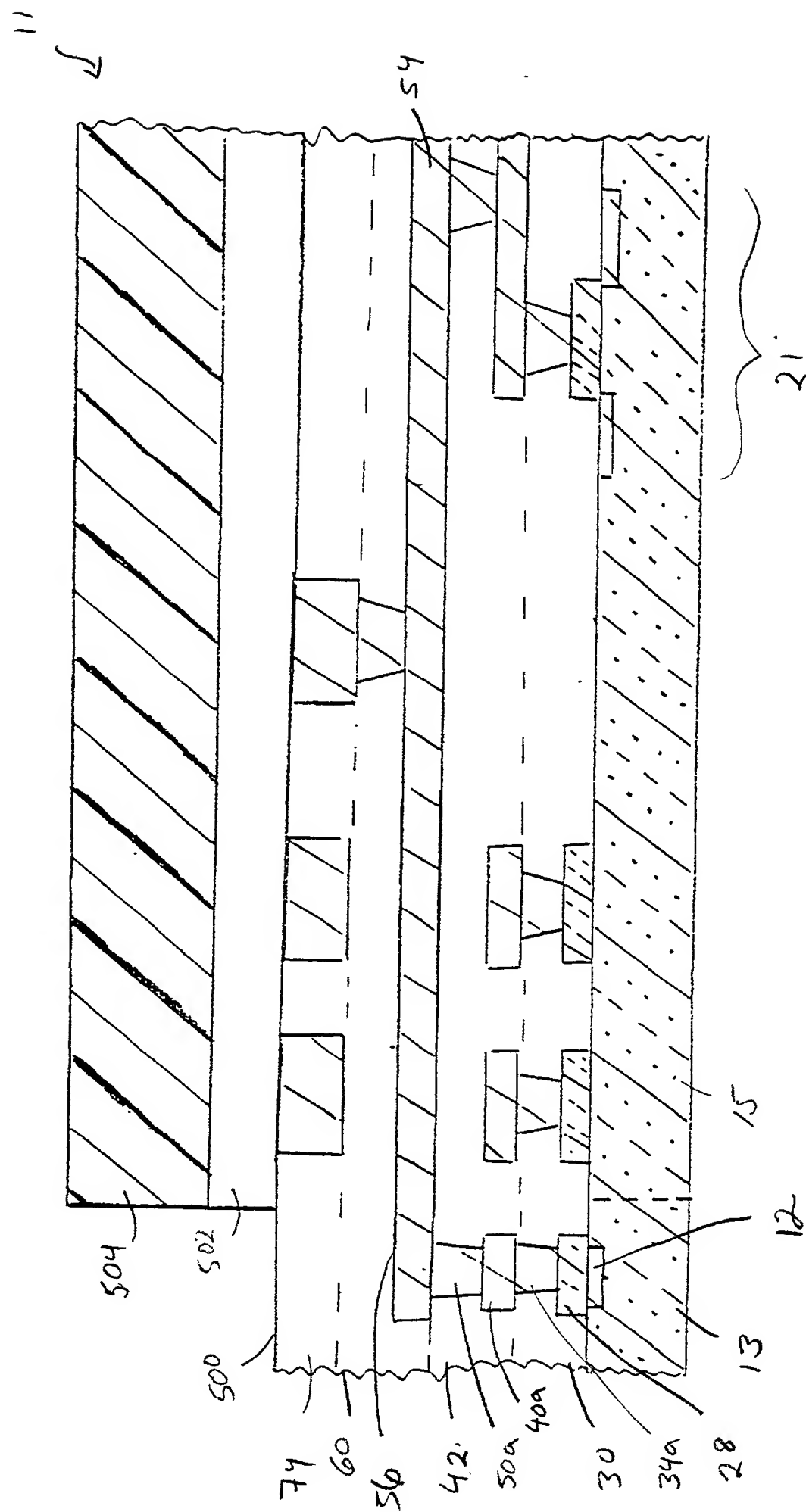


Fig. 12

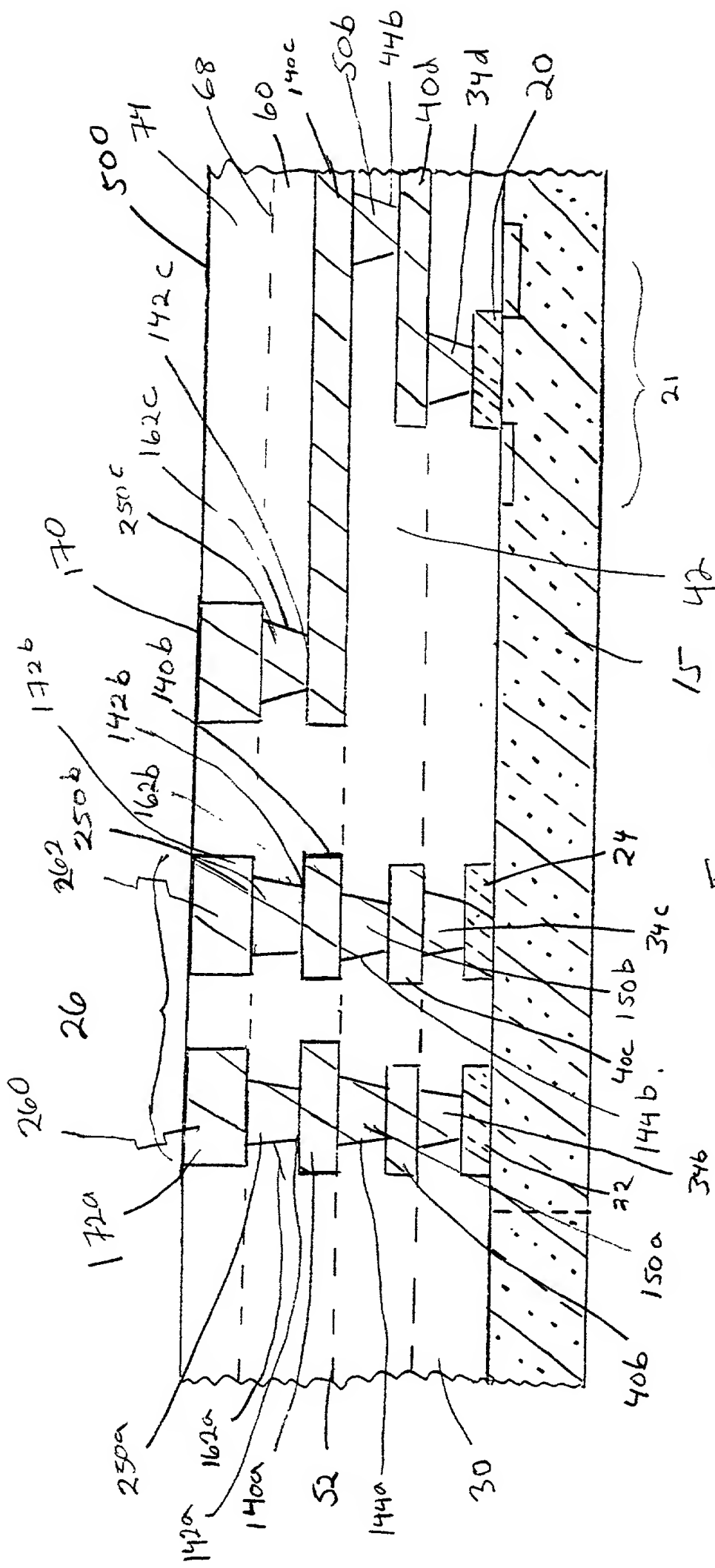


Fig. 13

FIG. 14 is a cross-sectional view of a device 100, showing a substrate 102, a first layer 104, a second layer 106, and a third layer 108. The first layer 104 is formed on the substrate 102, and the second layer 106 is formed on the first layer 104. The third layer 108 is formed on the second layer 106. The first layer 104, the second layer 106, and the third layer 108 are formed in a patterned manner. The first layer 104, the second layer 106, and the third layer 108 are formed in a patterned manner. The first layer 104, the second layer 106, and the third layer 108 are formed in a patterned manner.

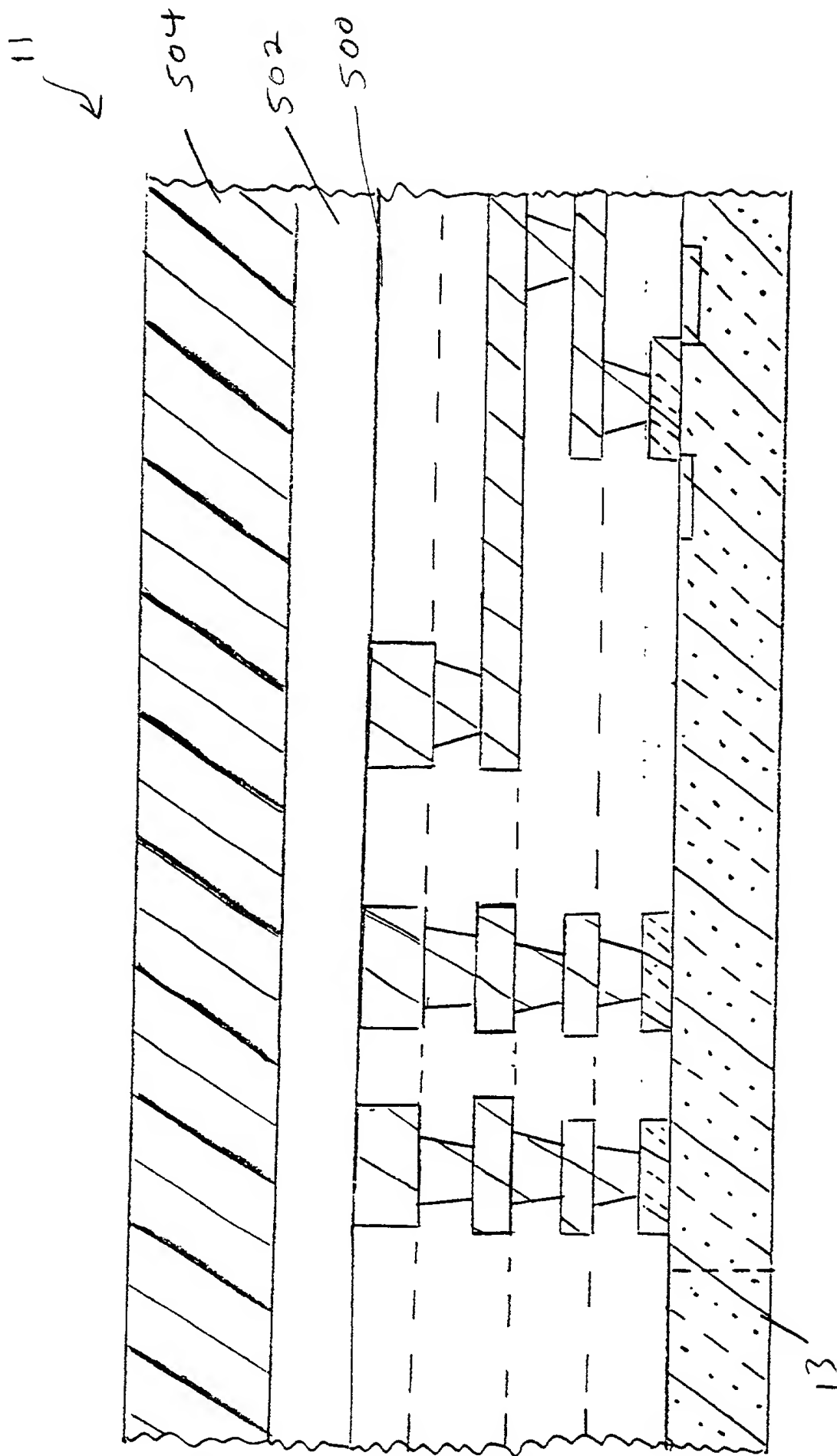


Fig. 14

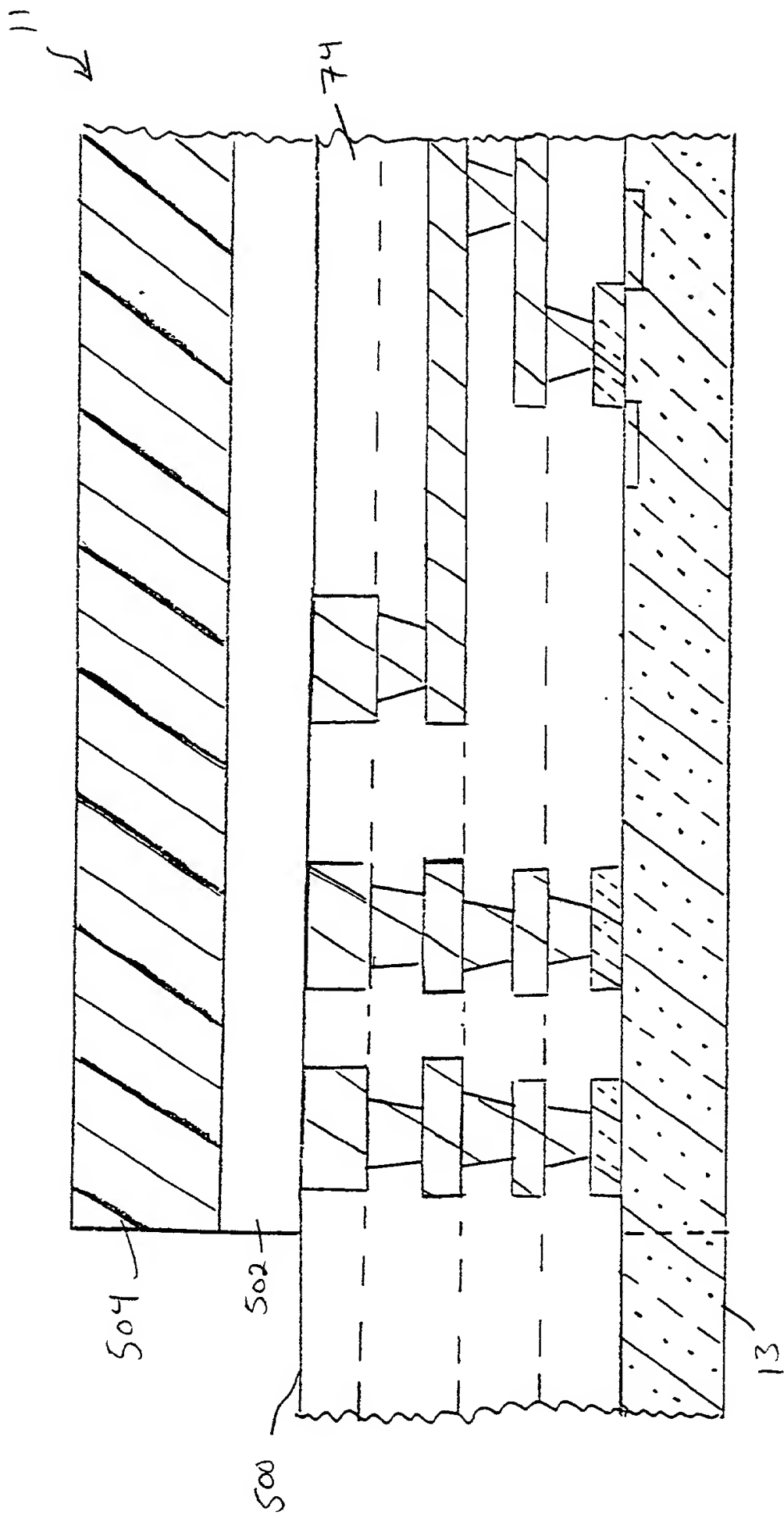


Fig. 5



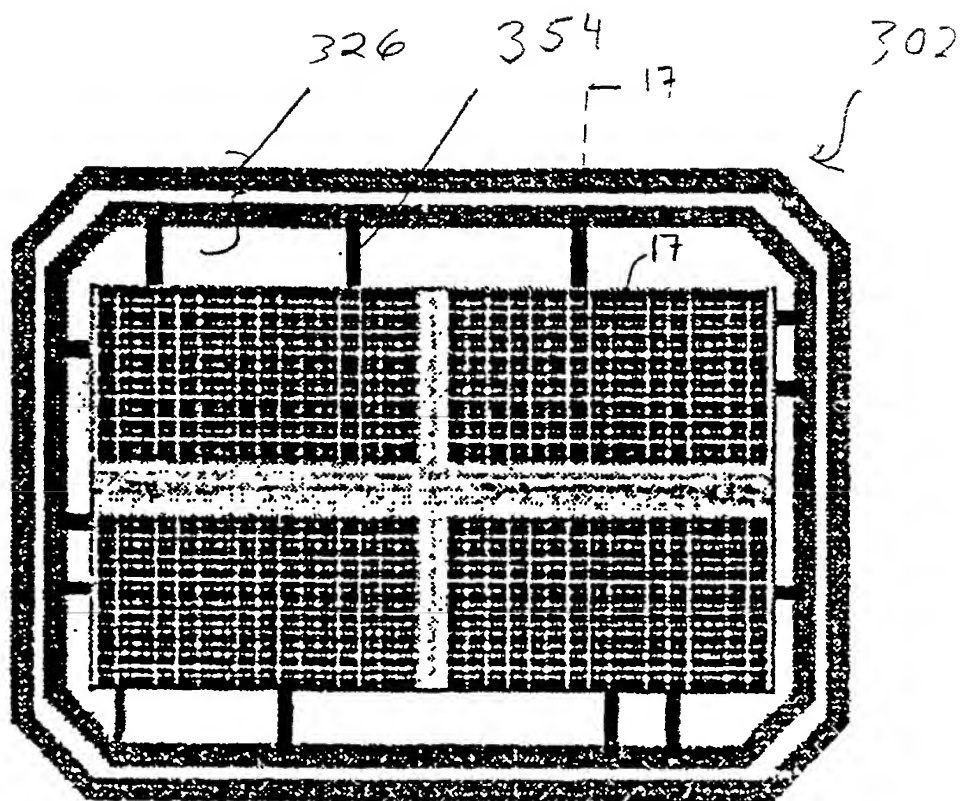


Fig. 16

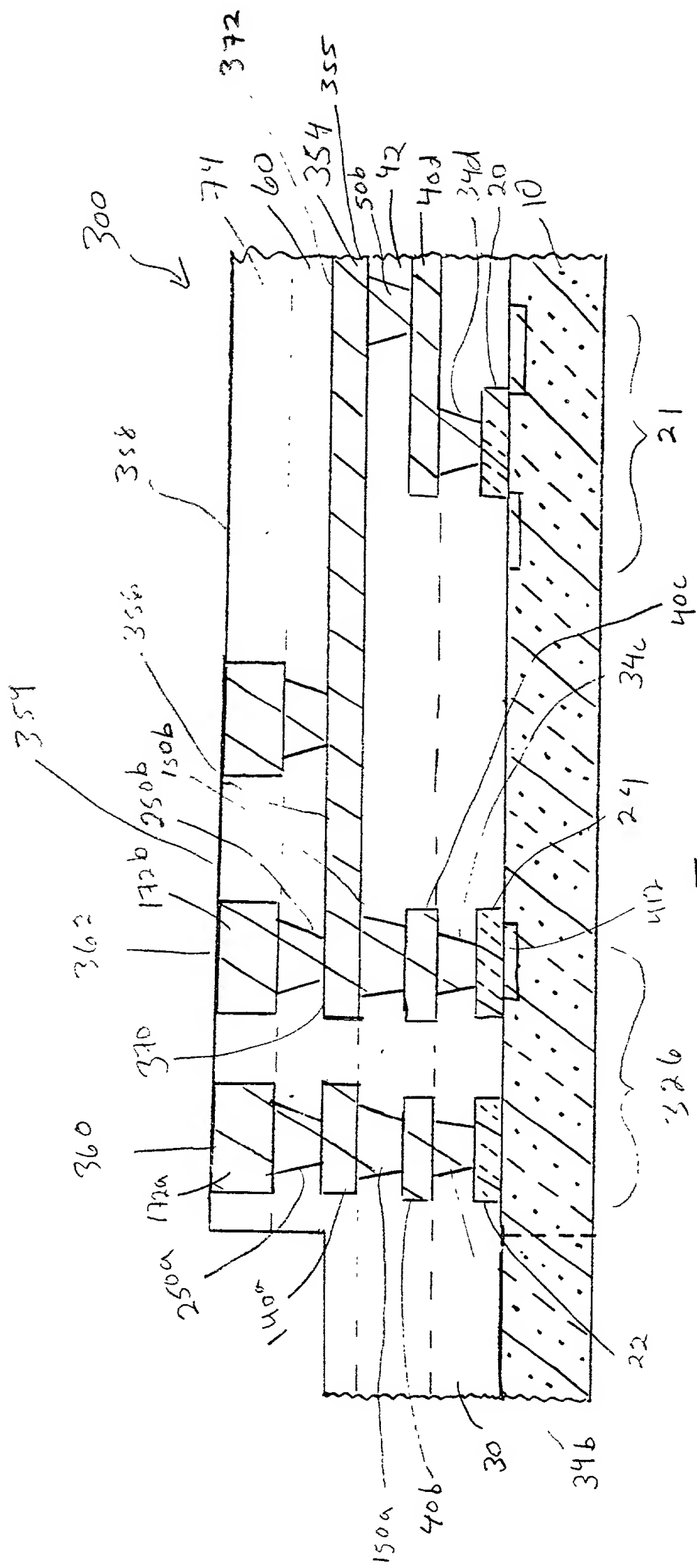


Fig. 17

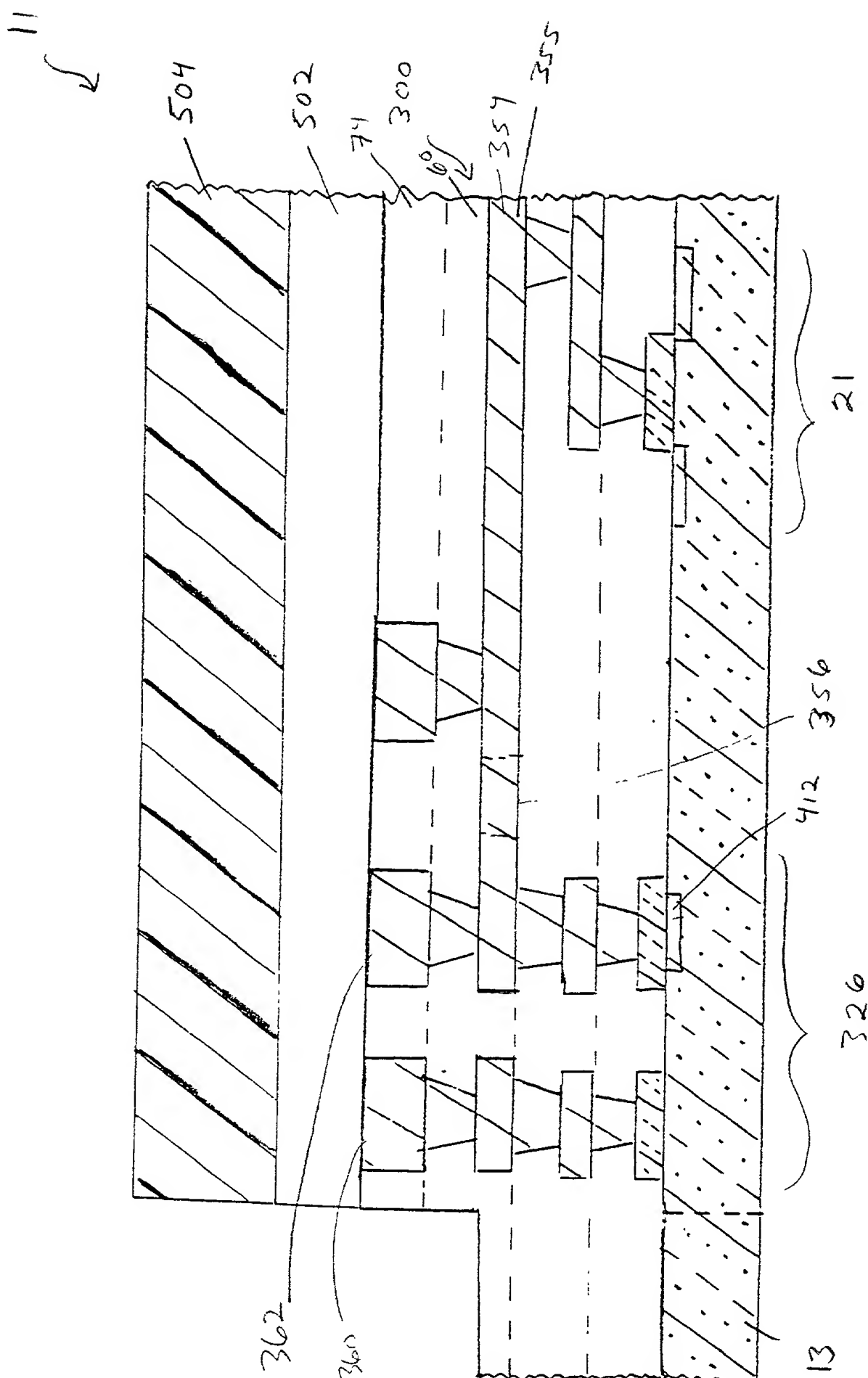


Fig 18

FIG. 19 is a cross-sectional view of a semiconductor device in accordance with the present invention. The device includes a substrate 10, a gate stack 11, a source/drain region 12, and a contact layer 13. The gate stack 11 is formed on the substrate 10 and includes a gate oxide layer 11a and a gate electrode 11b. The source/drain region 12 is formed in the substrate 10 and is electrically connected to the gate electrode 11b. The contact layer 13 is formed on the source/drain region 12 and is electrically connected to the gate electrode 11b.

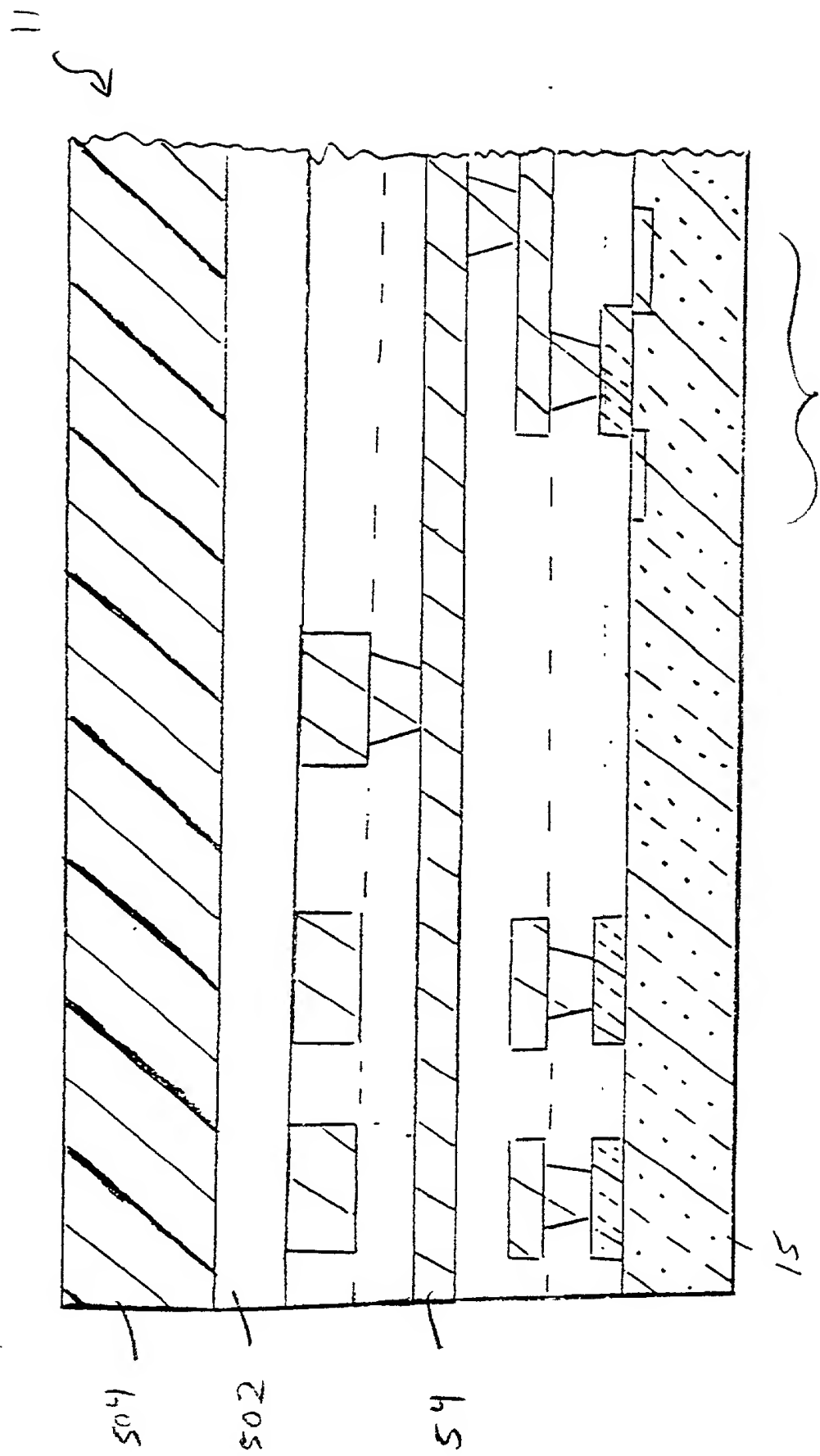


Fig. 19

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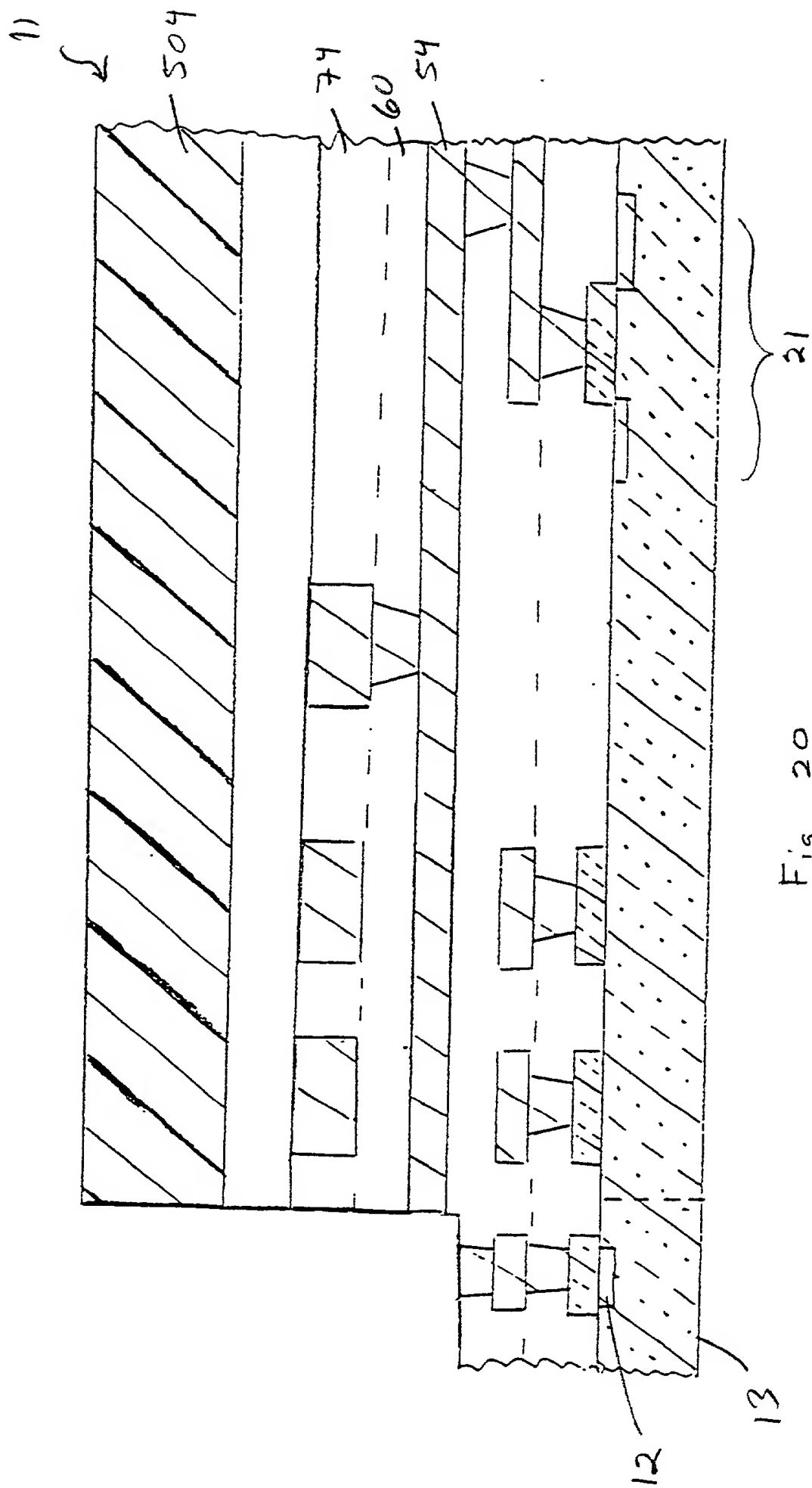


Fig. 20

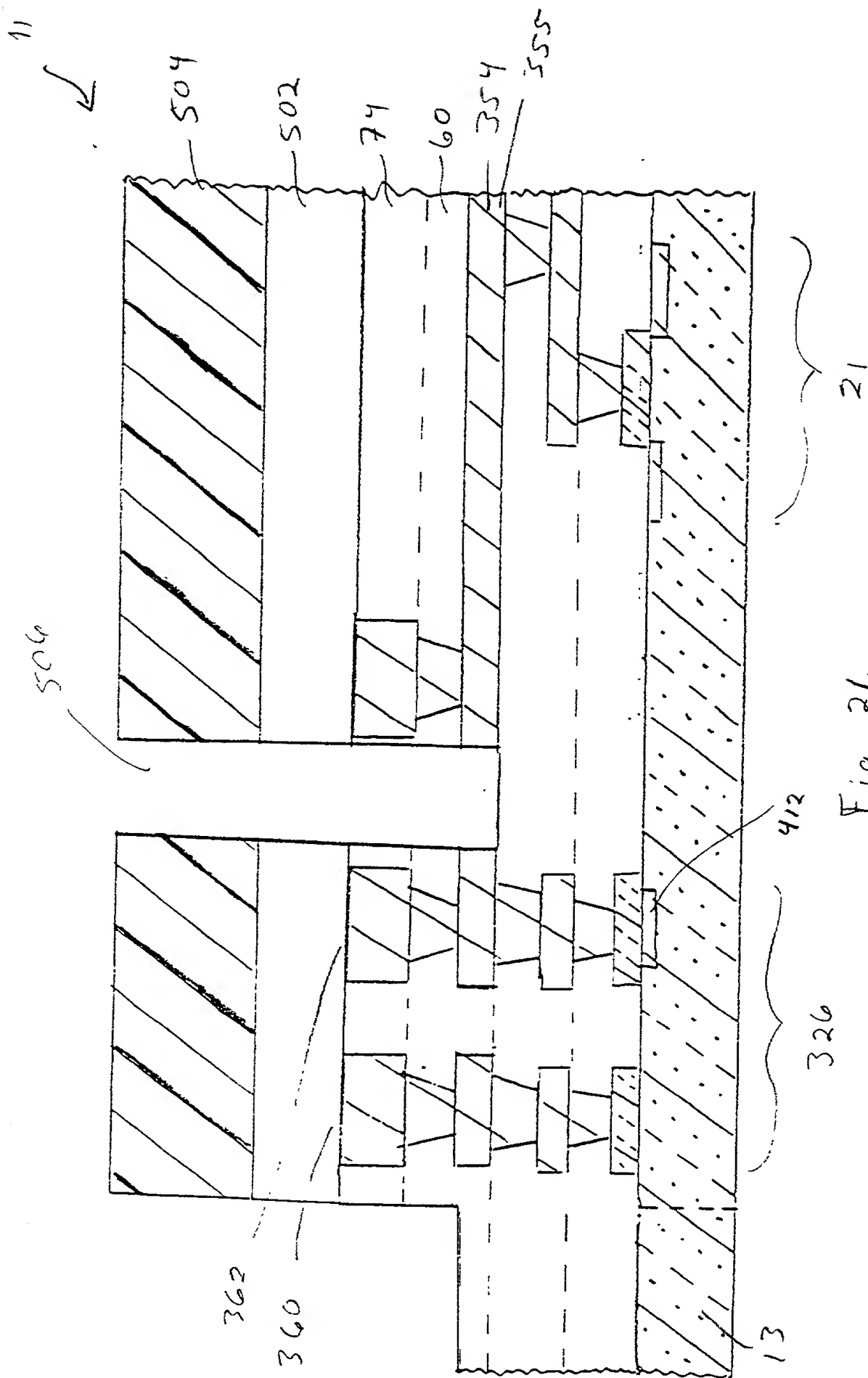


Fig. 21.